Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Original) A semiconductor memory device comprising a plurality of memory cells each comprising:

first to fourth wells formed on a semiconductor substrate and isolated from one another;

a first MOSFET of a first conductive type formed in said first well, having a diffused layer becoming a drain and connected to one of a pair of bit lines, and having a gate connected to a word line;

a second MOSFET of the first conductive type formed in said first well, having a

diffused layer becoming a drain, the diffused layer being a common diffused layer becoming a source of said first MOSFET;

a third MOSFET of the first conductive type formed in said second well, having a diffused layer becoming a drain and connected to the other bit line of the pair of bit lines, and having a gate connected to said word line;

a fourth MOSFET of the first conductive type formed in said second well, having a diffused layer becoming a drain, the diffused layer being a common diffused layer becoming a source of said third MOSFET;

a fifth MOSFET of a second conductive type formed in said third well, and having a gate common to the fifth MOSFET and said second MOSFET;

a sixth MOSFET of the second conductive type formed in said fourth well, and having a gate common to the sixth MOSFET and said fourth MOSFET;

a first wiring connecting a diffused layer becoming a source of said second MOSFET to a diffused layer becoming the drain of said fifth MOSFET;

a second wiring connecting a diffused layer becoming a source of said fourth MOSFET to a diffused layer becoming a drain of said sixth MOSFET;

a first contact section formed in an isolation region isolating said first well from said third well, and connecting said first wiring to the gates of said fourth and sixth MOSFET's; and

a second contact section formed in an isolation region isolating said second well from

said fourth well, and connecting said second wiring to the gates of said second and fifth MOSFET, wherein said first well is connected to said third well through the gates of said second and fifth MOSFET's, and

said second well is connected to said fourth well through the gates of said fourth and sixth MOSFET's.

10. (Original) The semiconductor memory device according to claim 9, wherein said first contact section and said second contact section are arranged to be opposed to each other.

11. (Original) The semiconductor memory device according to claim 9, wherein the diffused layers becoming the sources of said first and third MOSFET's are L-shaped.